Synthesis of IJTAG Networks for Multi-Power Domain Systems on Chips

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***Abstract*—The high-volume manufacturing test ensures the production of defect-free devices, which is of utmost importance when dealing with safety-critical systems. Such a high-quality test requires a deliberately designed scan network to provide a time and cost-effective access to many on-chip components, as included in state-of-the-art chip designs. The IEEE 1687 Std. (IJTAG) has been introduced to tackle this challenge by adding programmable components that enables the design of reconfigurable scan networks. Although these networks reduce the test time by shortening the scan chains' lengths, the reconfiguration process itself incurs an additional time overhead. This paper proposes a heuristic method for designing customized multi-power domain reconfigurable scan networks with a minimized overall reconfiguration time. More precisely, the proposed method exploits a-priori given non-functional properties of the system, such as the power characteristics and the instruments' access requirements. For the first time, these non-functional properties are considered to synthesize a well-adjusted and highly efficient multi-power domain network. The experimental results show a considerable improvement over the reported benchmark networks.**

***Index Terms*—IEEE 1687 Std., IJTAG design, Test Scheduling, Multi-power Domains, Reconfigurable Scan Networks, Scan Network Design**

I. Introduction

The IEEE 1687 Std. (IJTAG) has been introduced to tackle the problem of long scan chains in modern *System on Chips* (SoCs). In order to provide efficient access, IJTAG exploits programmable components such as *Segment Insertion Bits* (SIBs) and *ScanMux Control Bits* (SCBs) to create reconfigurable scan networks [1]. By using these elements, IJTAG enables the reduction of test time through hierarchical networks by excluding the redundant segments in the test sessions. However, this flexibility comes at the cost of an additional reconfiguration time. Several research works have been carried out that address this problem [2]–[17]. Some of these works have investigated structural modifications for test time reduction, like [10], [11], [13]. In work [6], the authors have presented new methods to minimize the reconfiguration process. Pseudo-Boolean Optimization is employed in [4], [5] to optimize the scan pattern generation and, hence, to reduce the test time. Besides the configuration time overhead, the access sequence of the instruments affects the overall test time significantly. Thus, the works [14]–[16], [18] have proposed approaches to reduce the test time by optimizing the test schedule. In summary, the design of a fully flexible *Reconfigurable Scan Network* (RSN) that provides access to all combinations of instruments will lead to excessive test time and area overhead as long as the given non-functional properties are not appropriately considered during the test network design. Besides the flexible instrument access, the implementation of multiple power domains in the state-of-the-art SoCs poses new challenges for RSN design such that neglecting this feature can result in effects like IR drop during the test application phase [19].

This paper proposes a design methodology for IJTAG networks allowing for a significant reduction of the test time by minimizing the configuration time overhead. In general, the intended test scenario, power consumption of individual instruments and, furthermore, the instruments' security and access requirements are a-priori known properties at early design phases. Consequently, this work exploits this information to improve the resulting scan network efficacy significantly. In particular, the proposed technique re-designs a given IJTAG network to improve its reconfiguration mechanism or to design IJTAG network from scratch based on a set of given constraints. The proposed framework considers the recent multi-power domain SoC design paradigms, dividing the SoCs into multiple power domains for improved power management [20]. Although security improvement as another goal of interest in IJTAG networks design is not the main objective of this work, the proposed method can provide secure access to designated instruments through synthesizing exclusive access chains [21]–[24].

The remainder of this paper is organized as follows: Section II gives a brief overview of IJTAG and the principle of access scheduling in scan networks. The proposed method is described in Section III. Furthermore, Section IV reports the experimental results and, finally, the paper is concluded in Section V.

II. Background

IJTAG scan networks have been introduced to tackle the problem of long scan chains in state-of-the-art SoCs by adding programmable components such as SIBs and SCBs, which enables the design of hierarchical and reconfigurable scan networks. The basic concept of IJTAG networks is shown

in Fig. 1(a). Four instruments divided into two power domains are connected to the network via parallel *Test Data Registers* (TDRs). The network includes five SIBs and one SCB as programmable components, which are all set to zero in the initial state. This implies that after initialization, the scan chain includes only SIB_1 and SCB_1. In order to access I_1 and I_2 concurrently, first the access to SIB_2 and SIB_3 should be granted by shifting $\{1, 0\}$ to the initial scan chain. In the next step, the scan pattern $\{1110\}$ activates the chain $\{SI \rightarrow SIB_1 \rightarrow SIB_2 \rightarrow I_1 \rightarrow SIB_3 \rightarrow I_2 \rightarrow SCB \rightarrow SO\}$ and enables the access to I_1 and I_2. The same process is used to access other instruments in the network.

In every access, the data is transferred to the instruments over *Capture Shift Update* (CSU) Cycles. Each CSU shifts one test pattern into the scan chain. A number of successive CSUs that include the same active instruments constitute an access session, as indicated by S_1-S_4 in Fig. 1(b). During a session, the network has a fixed configuration and, hence, the scan chain remains unchanged. All TDRs included in the active chain can concurrently exchange the data with their corresponding instruments.

For enabling an efficient access to instruments through an IJTAG network, test schedulers are required that consider the individual instruments' constraints and are compatible with recent multi-power domain chip design paradigms. The framework proposed in [16] is an instance of such a scheduler that employs formal techniques to provide an optimized access schedule based on power, access, and structural constraints. Fig. 1(b) illustrates an example of a test schedule for the network shown in Fig. 1(a) according to the given scenario. Information about the power domain, power consumption, and number of required access or test pattern for every instrument are provided in the table.

The access scenario in Fig. 1(b) is scheduled in four sessions over six CSUs. Besides the power constraints and the required number of test patterns, an access plan can embrace other constraints regarding the accessibility of elements. For example, two instruments can be bound to be accessed only together, or on the contrary, they can be scheduled for more secure access over exclusive scan chains.

III. Proposed IJTAG design methodology

This section describes an efficient RSN design methodology that does not modify the standard elements of the scan network, as defined in IEEE 1687 Std. Algorithm 1 summarizes the proposed method. Since the instruments accessed by IJTAG networks are previously designed embedded cores, their specifications such as power consumption or test methods are already known during the IJTAG network insertion. Given a list of instruments, their power characteristics, and accesses requirements as the inputs, the developed framework incorporates this information into an optimized access plan (Line 1). Subsequently, the calculated schedule is sorted in ascending order to give priority to the sessions with the fewer number of instruments. Next, the instruments in every session are sorted in descending order, giving priority to those that appear in more sessions (Line 2). This increases the probability of placing these

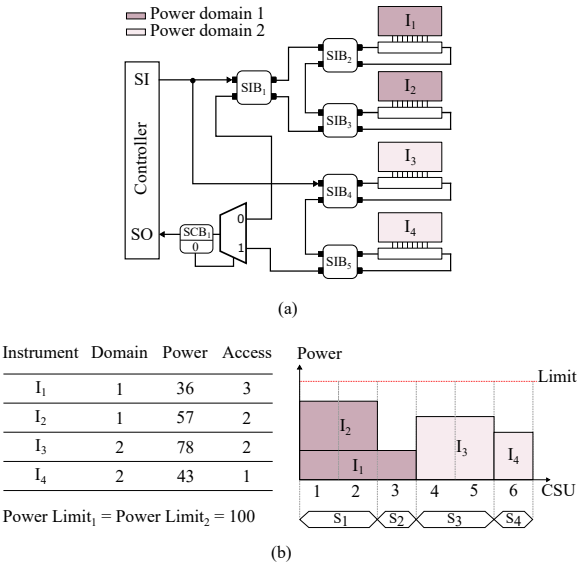

Fig. 1. (a) Example of an IJTAG network; (b) Instrument access schedule for network (a) based on given constraints

instruments as branching nodes. The synthesis is implemented session by session in two main phases. First, those instruments of the session that are already available in a stack are collected to create a directed path according to their order in the stack (Lines 6-11). This prevents the creation of cycles in the graph. In the next phase, the remaining instruments of the session which are in descending order are added to the path and then are saved in the stack to be used in the next sessions (Lines 13-18). The following subsections explain in detail how to set up an access strategy that is next used to create a tailored network that avoids unnecessary time overhead.

A. Access Plan

The proposed framework creates an optimized access plan to ensure a minimized number of CSUs that fulfill all instruments' access requirements. This plan considers the design's power specifications namely power domains' limits and the power consumption of the integrated instruments. Accordingly, the objective function is defined as a pseudo-Boolean optimization problem as

$$Min \sum_{s \in \mathcal{S}} CSU_s \tag{1}$$

which minimizes the overall CSUs required to access all instruments and is subject to the power and access constraints as follows:

$$\bigwedge_{\forall s \in \mathcal{S}} \bigwedge_{\forall d \in \mathcal{D}} \left(\sum_{p_i \in d} p_i \leq P_{max,d} \right) \tag{2}$$

$$\bigwedge_{\forall i \in \mathcal{I}} \sum_{s \in \mathcal{S}} a_{i,s} = A_i \tag{3}$$

Where $\mathcal{S}$ and $\mathcal{D}$ in (2) represent the set of sessions and power domains, respectively. p_i refers to the power consumption of i-th active instrument in domain d of session s. Constraint (2) ensures that the power consumption in each session does not exceed the allowed power limits. The second constraint given

Algorithm 1: Proposed RSN design procedure

Input: *power constraints, access constraints*
Output: *RSN with minimized configuration time overhead*

schedule = calcSchedule(*power constraints, access constraints*)
sortSchedule(*schedule*)
S = Number of sessions
K = Number of elements in stack
for *(s=0 to S-1)* **do**
    // Add the instruments available in the stack
    for *(k=0 to K-1)* **do**
        if *stack[k]* ∈ *session[s]* **then**
            scanChain[s] ← *stack[k]*
        end
    end
    // Add the remaining instruments
    for *i=0 to session[s].size()* **do**
        if *s[i]*∉*stack* **then**
            scanChain[s] ← *s[i]*
            stack ← *s[i]*
        end
    end
end
function CalcSchedule(*x,y*)**:**
    Calculate an optimized access plan based on x and y requirements.
return
function sortSchedule(*given schedule*)**:**
    Sort the given schedule in ascending order.
    Sort every session in descending order.
return

by (3) implies that every instrument from the set of instruments $\mathcal{I}$ will be accessed A_i times over the scheduling plan.

Although the proposed method targets the creation of a network with optimized access time, two extra constraints are added to provide secure and bound access to designated instruments. Assuming S_i and S_j as sessions that include the instruments i and j, the exclusive access is defined to provide secure access according to the following constraint:

$$\bigwedge_{\substack{\forall i \in \mathcal{Q}, \\ j \in \{\mathcal{I}-i\}}} S_i \cap S_j = \varnothing \tag{4}$$

where $\mathcal{Q}$ is the set of instruments that require secure access. The last constraint ensures that a set of bound instruments $\mathcal{B}$ are accessed only together in the same session s:

$$\forall i, j \in \mathcal{B} : (i \in s) \Leftrightarrow (j \in s) \tag{5}$$

For a better understanding and evaluation of the proposed method, the resynthesis of the Mingle network from ITC'16 benchmark suite is described in the remainder of this section.

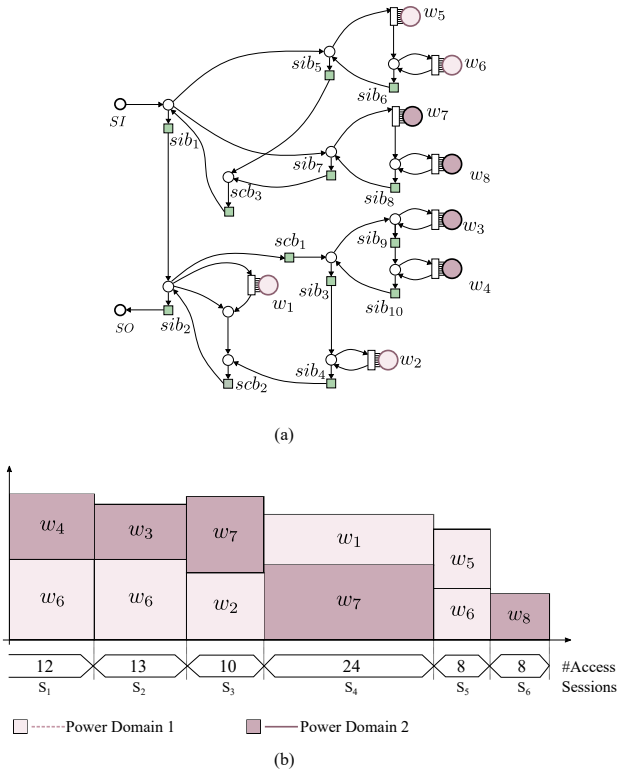

Fig. 2. (a) Graph representation of the Mingle network. (b) Example of an access plan calculated by the framework for a given set of constraints.

Fig. 2(a) shows the graph representation of the Mingle network. As defined in [14], SIBs should be modeled with two vertices; however, for the sake of a more comprehensible presentation, they are merged into one node in Fig 2(a). Nevertheless, it should be noted that SIBs do not allow the creation of cycles in the graph. The instruments w_1 to w_8 are divided into two power domains and are accessible via ten SIBs and three SCBs which are indicated by small squares. These configuration bits control the scan multiplexers which are represented by white nodes in the figure.

Fig. 2(b) shows an instance of an access schedule compatible with this network which is generated to be used during the network resynthesis process. An exclusive access to the instrument w_8 is also intended. The table of power and access constraints is omitted in this figure. However, it is assumed that this access plan satisfies the given constraints.

B. Network Synthesis

This section describes how the calculated schedule is exploited to design a scan network with reduced access overhead. In order to calculate the configuration time overhead, first, the number of configuration bits used in every scan session should be counted. Likewise, redundant TDRs that are not intended for accessing during the corresponding session are considered as configuration overhead. With every access during a CSU, these local overheads are added to the overall time overhead. The final value is obtained by accumulating the calculated clock

cycles over the all test sessions.

$$C_{total} = \sum_{s \in \mathcal{S}} CSU_s \cdot (C_s + TDR_s) \tag{6}$$

Where C_{total} is the overall configuration overhead and CSU_s and C_s are the number of CSUs and configuration bits in session s respectively. TDR_s represents the number of redundant scan registers in session s. Accordingly, the optimization's objective is defined as:

$$Min\{C_{total}\} \tag{7}$$

Every scan chain in an IJTAG network establishes a path between SI and SO, which includes the instruments that should be accessed during the current test session. Since IEEE 1687 Std. considers the creation of loops in IJTAG as a bad design practice, the scan network is assumed to follow a directed acyclic graph model. Based on the serial attribute of the regular IJTAG networks defined in the standard, every merging point in the graph implies the presence of a scan multiplexer that selects one of the input paths. In contrast, branches do not introduce any additional components and, hence, do not incur any hardware overhead. The proposed method sorts the calculated schedule in ascending order, from sessions with the fewest number of instruments to those containing the highest one. This reduces the randomization of instruments' orders in the next steps during the creation of scan chains. A second descending sorting in every session prioritizes the placement of nodes with a higher number of neighbors. This ensures the creation of branches instead of multiplexers and hence, contributes to the reduction of area overhead. As an example, for the initial unsorted schedule given in Fig. 2(b) the sorted schedule would be $\{(w_8), (w_6, w_4), (w_6, w_3), (w_6, w_5), (w_7, w_1), (w_7, w_2)\}$.

After sorting, the process continues for each session by creating a chain that starts from SI, covers all instruments of the corresponding session, and finally ends at SO. To ensure a cycle-free network a stack is used to keep track of the topological order of the nodes. Every instrument of the current session is compared with previous elements of the stack before being added to the graph. This is to ensure the creation of unique vertices. The new node is also added to the stack and updates the instruments' sequence, which should be followed in the next sessions. As an example, in Fig. 3, the first session only includes w_8 which is a new node and therefore an exclusive branch is generated for it. Similarly, in the next step, w_6 and w_4 as new nodes are added to the network on the same branch and the stack is updated accordingly. w_6 enters the stack before w_4 since despite w_4 which only has been accessed in one session, w_6 appears in three different sessions and thus has a greater degree. In Fig. 3(c) which schedules $\{w_6, w_3\}$, w_6 is already available in the network and therefore only w_3 will be added to the stack. Consequently, the chain $\{\text{SI} \rightarrow w_6 \rightarrow w_3 \rightarrow \text{SO}\}$ is created by branching the previous chain. Henceforth, every session that includes w_6 and w_3 has to follow the same sequence that is saved in the stack. Otherwise, a cycle will be created. The process continues until the generated network covers all sessions. Fig. 3(f) shows the completed graph. Six branches are merged at the output of the network. This necessitates a multiplexer with three control bits or SCBs on the scan path.

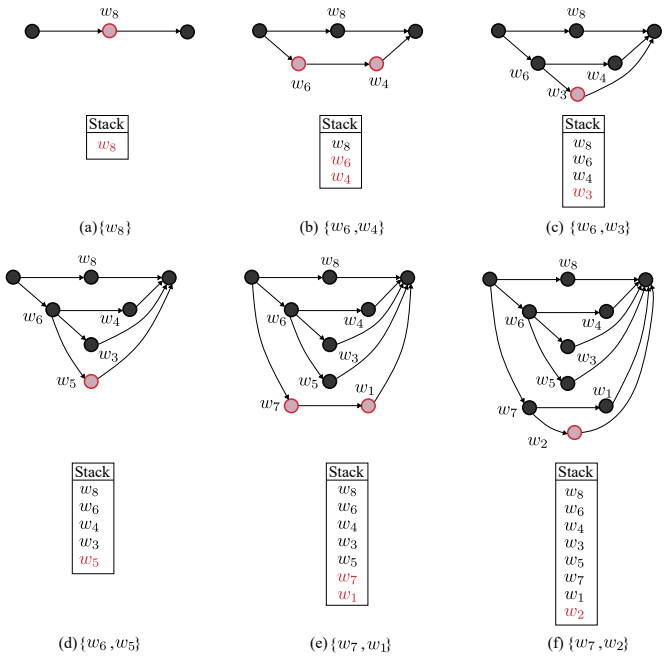

Fig. 3. RSN graph design procedure for the Mingle network based on the schedule given in Fig. 2(b)

According to (6), the configuration overhead of the Mingle network for the schedule given in Fig. 2(b) is calculated as $589{+}25{\cdot}TDR_5{+}8{\cdot}TDR_7$. As depicted in Fig. 2(a), TDR_5 and TDR_7 are redundant elements that cannot be excluded from the scan chain when accessing w_6 and w_8 over the sessions s_1, s_2, and s_6. By assuming a minimum length of 1 bit for the TDRs, the total time overhead of Mingle network for its optimized schedule is calculated as 622 clock cycles. However, the configuration overhead of the generated network using the same equation is calculated as 225, which shows a considerable reduction in comparison to the benchmark network.

As shown in Fig. 4, the design is further improved by removing the SCBs from the instruments' scan paths and implementing them as remote controllers on a separate branch. This eliminates the time overhead due to shifting the configuration bits alongside the instrument data bits in every CSU. The only excessive configuration data is due to a one-bit mode selection register which is labeled as c_1 in Fig. 4. This register enables switching between configuration mode and instruments' data mode over one clock cycle. In this network, every session includes two separate configuration and scan phases. The test process starts by initializing the network to the configuration mode. The required network configuration for the first session is shifted to the configuration branch, plus one extra bit for changing the state to the scan mode. Upon receiving an update signal from the controller, a new scan chain that is customized for the current session is established. In order to keep the network in scan mode or switch it to the configuration mode at the end of sessions, one bit is concatenated to every test pattern, which is updated to the mode selection register with every CSU. Some control signals have been omitted from Fig.4 to

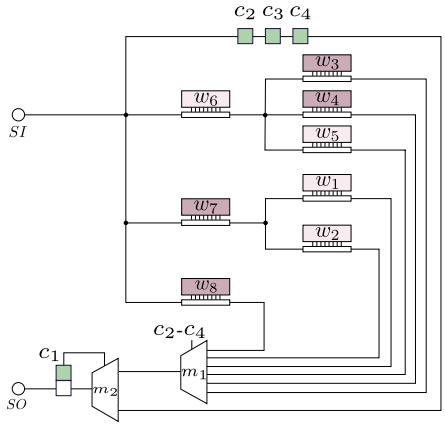

Fig. 4. Generated scan network based on the constraints given in Fig. 2(b)

simplify the illustration. The overall configuration overhead in the proposed method is calculated using the following equation:

$$C_{total} = S \cdot (C + 1) + CSU \tag{8}$$

The first part of the equation is due to the overall overhead in configuration mode. S is the number of sessions and C represents the total number of remote configuration bits which is the same for all sessions. The second part concerns the sum of mode selection overhead in scan mode over the all CSU cycles and is referred to as CSU. According to this equation, the total overhead for the proposed network is calculated as 99 clock cycles which shows about 84% reduction compared to the Mingle network for the given optimized schedule. Besides improving the overall access time, the generated network provides more secure access to instrument w_8 by assigning an exclusive chain which consequently prevents another instrument from accessing w_8's data. From a circuit implementation perspective, it should be noted that for larger networks the proposed method will not necessarily create one scan multiplexer with numerous inputs. Instead, the synthesis process will introduce more scan multiplexers inside the network.

IV. Experimental results

This section evaluates the efficacy of the proposed approach by considering multiple benchmark candidates. In order to implement the proposed method, a framework has been developed in C++. The experiments have been conducted on a machine holding an *AMD Ryzen 7 PRO 4750U* processor and 16GB of main memory. For a precise evaluation of the proposed approach, the results are compared with the performance of ITC'16 IJTAG benchmark networks [25] given in Table I. The number of instruments included in every network is given in column (2). Different scenarios are designed that divide these instruments into multiple power domains that are mentioned in column (3). The power consumption of the instruments and the power limit of every domain are generated randomly and a random number of required access or test patterns are assigned to every instrument. Column (4) shows the number of configuration bits in the benchmark networks which include the registers inside SCBs and SIBs. Based on the defined scenarios, optimized access schedules are calculated to ensure a minimized overall instrument access time for the given networks. The resulting overall access time overheads that are shown in column (7) are the minimized values that can be achieved for the calculated schedules using the benchmark networks' structures.

In order to show that the proposed method can satisfy the same access plan with lower overall time overhead, the calculated schedules have been sorted and used to resynthesis the scan networks. Consequently, the structural constraints of the benchmark are imposed on proposed networks as well to provide an impartial comparison in the same conditions. In other words, the obtained values for the proposed method can be even further improved when exclusive schedules –without structural constraints– are calculated for them. Column (5) reports the resulting number of configuration bits generated by the proposed framework. The networks' size changes in percent are presented in column (6). Negative values indicate a reduction of the network size in comparison to the benchmark. Since reducing the hardware overhead is not the primary target of this work, the proposed method does not guarantee the creation of networks with a minimum number of configuration registers. In fact, the number of configuration bits has been improved for many of the benchmarks. It should be noted that the major part of the area overhead induced by RSNs is due to the multi-bit TDRs, which remain unchanged in the synthesized networks. The results show a significant reduction of the overall access time overhead for all considered benchmarks (column 8) compared to the initial benchmark networks' values (column 7), as primarily targeted by this work. More precisely, for the same access plan as the benchmark networks, the proposed framework has achieved a significant reduction rate in the overall access time overhead, as presented in column (9).

V. Conclusion

This paper proposed a method for designing reconfigurable scan networks that contributes to the test cost reduction through minimizing the reconfiguration time overhead. This was accomplished by employing a-priory known information about the power plans and test scenarios in terms of the intended test schedules. More precisely, a framework was developed that combines the power and access requirements for creating a highly effective access scenario. This scenario was then used as the basis for generating a customized reconfigurable scan network. In the end, the proposed technique provides a scalable solution that can be used to create networks with thousands of instruments, as proven by the experimental results, Future works can consider optimization techniques to further improve this method by reducing the area overhead or more optimized methods of graph generation.

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TABLE I
COMPARING THE GENERATED IJTAG NETWORK WITH ITC'16 BENCHMARK NETWORKS

(1) **Network**	**(2) #Instruments**	**(3) #Domains**	**Configuration area overhead [bits]**			**Access time overhead [clk]**		
			(4) ITC'16	(5) Proposed	(6) Network size %	(7) ITC'16	(8) Proposed	(9) Reduction rate %
Mingle	8	3	26	9	-11.04	986	197	-80.02
BasicSCB	5	3	20	4	-16.00	1016	163	-83.96
TreeFlat	11	3	26	15	-5.45	2120	280	-86.79
TrapOrFlap	12	3	24	13	-5.09	2390	356	-85.10
q12710	23	4	54	27	-6.40	4533	854	-81.16
a586710	22	4	64	27	-8.89	5637	766	-86.41
t512505	128	6	318	307	-0.46	57093	35929	-37.07
p22810	242	7	540	647	2.43	163214	138080	-15.40
p34392	73	7	194	135	-4.33	27759	9193	-66.88
N17D3	27	3	30	29	-0.22	9360	1351	-85.57
N32D6	44	4	46	70	3.20	12359	3215	-73.99
N73D14	90	5	92	193	6.59	56797	17801	-68.66
N132D4	172	5	158	389	7.94	187261	63590	-66.04
NE600P150	793	6	802	2345	11.44	2043203	1647285	-19.38
NE1200P430	1629	7	1622	5213	12.97	9839190	7464753	-24.13

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