Hidden Cost of Circuit Design with RFETs

Sajjad Parvin[ψ], Chandan Kumar Jha[ψ], Frank Sill Torres[‡], and Rolf Drechsler[ψ,†]
[ψ] Institute of Computer Science, University of Bremen, Germany
[†] Cyber-Physical Systems, DFKI GmbH, Germany
[‡] Institute for the Protection of Maritime Infrastructures, German Aerospace Center, Germany
{parvin, chajha, drechsler}@uni-bremen.de, frank.silltorres@dlr.de

***Abstract*—Reconfigurable Field Effect Transistors (RFETs) can be programmed on the fly to behave either as NMOS or PMOS. Digital circuit designs using RFETs have been shown to benefit both in design and security metrics compared to traditional FETs. In this paper, we highlight the problem associated with the cascading of RFET-based logic cells that have their Source(S)/Drain(D) terminals not connected to the supply Voltage(VDD)/Ground(GND). While these circuits occupy a lesser area, there is a drastic increase in the delay of these logic cells when they are cascaded as a result of the S/D being driven by inputs. We then discuss two methods to mitigate this issue using a) buffer insertion for delay minimization, and b) logic cells that have their S/D terminals driven by VDD/GND.**

***Keywords*—Reconfigurable Field Effect Transistor, emerging technologies, mirror adders, ripple carry adders.**

I. Introduction

Reconfigurable Field Effect Transistors (RFETs) are being extensively explored for implementing digital circuits. One type of RFET called *Three-Independent-Gate Field-Effect Transistor* (TIGFET) is shown in Fig. 1 [1]. They can be configured at runtime to be either p-type/n-type transistors to implement multi-functional designs [1]. Also, as a result of reconfigurability the area required for building these designs is much lower as compared to using traditional (non-configurable) transistors [2]. Since these circuits give notable benefits in the area, most of the prior works are focused on minimizing the area of the digital circuits using RFETs [2].

While the configurable designs implemented using RFETs are suitable for implementing multi-functional designs, they come with some hidden costs. This was not evident from prior works as they limited the evaluation to only single-level gates [1], [3], [4]. In this work, we will show the deterioration in the performance when these single-level gates are cascaded, i.e., when multi-level circuits are implemented using these single-level gates. To achieve the lower area, a design technique called the *Gate Diffusion Input* (GDI) is used for RFETs, where the S/D terminals are driven by some inputs and not the supply Voltage(VDD)/Ground(GND) [5]. However, when GDI-based designs are connected in series, they form an *Resistor-Capacitor Ladder* (RC-Ladder) as shown in Fig. 2 which leads to a significant increase in the delay. In this work, we highlight this in state-of-the-art RFET designs and also propose solutions to mitigate it. *Our contributions:*

- We use an 8-bit *Ripple Carry Adder* (RCA) to highlight the increase in delay as a result of cascading in RFET-based logic cells whose S/D terminals are driven by inputs.
- We highlight the reason behind the drastic increase in delay of the RFET-based logic cells.
- Lastly, we examine two solutions for the problem, by a) inserting buffers and b) using traditional CMOS-based design techniques to improve the delay.

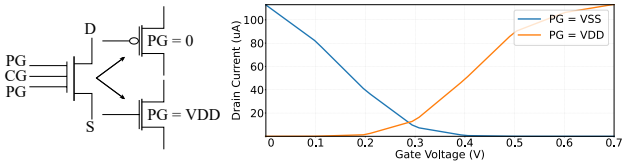

Fig. 1: Three-Independent-Gate Field-Effect Transistor (TIGFET)

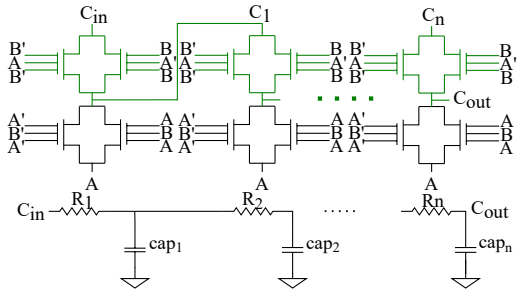

Fig. 2: Cascading of Carry Circuit for an n-bit RCA and the Associated RC Ladder

II. Issues with Cascading in RFETs

We have used the open-source TIGFET 10 nm model for our experiments [1]. The nominal supply voltage (VDD) is set to 700 mV. We evaluate the design of an 8-bit RCA as it is one of the fundamental designs in digital circuits. The input pattern is defined as A = 00000000, B=11111111, and C_{in} is made to transition from 0 to 1 because then the carry is propagated from the first stage to the last stage. Thus, this input pattern gives the largest delay. For every simulation, we have used a duty cycle of 0.4 to show all the carry signal waveforms, as some of the carry signals have a large delay.

A. RCA with Optimum RFET-based Full Adders

For the carry design, we use the state-of-the-art RFET-based design that utilizes only 4 transistors, as shown in Fig. 2 [3]. We highlight the hidden cost in terms of delay deterioration using this design. In this design, there is no power rail, and S/D of RFETs are used as an input signal similar to GDI. While the design works perfectly for *Full Adders* FA, the issue arises when this FA is used to implement an 8-bit RCA. Since the carry output of one stage is used as an input for the next stage, it forms a cascade of transistors in series. This cascading can be modeled using the RC ladder as shown in Fig. 2. For an RC ladder [6], the delay (D) of the carry at the n^{th} stage can be approximated using the Elmore delay model by

$$D = R_1 * cap_1 + (R_1 + R_2) * cap_2 + ... + (R_1 + R_2 + ... + R_n) * cap_n \quad (1)$$

Here, R_n and cap_n, are the resistance and capacitance of the n^{th} stage, respectively. As a result, delay degradation is caused by cascading these FAs, particularly in the carry signal path.

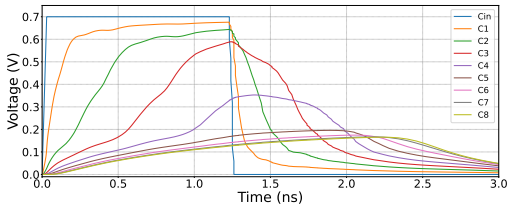

Fig. 3: 8-bit RCA without Buffers (Delay not shown, as outputs do not reach VDD)

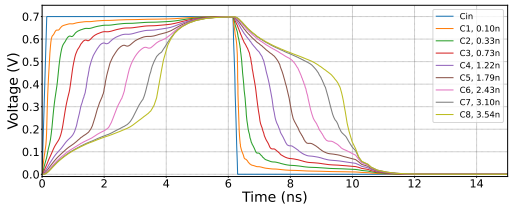

Fig. 4: Delay of carry Outputs of 8-bit RCA with Increased Time Period of 15 ns

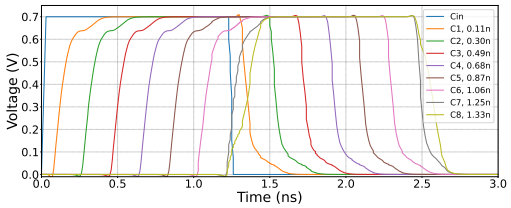

Fig. 5: Delay of Carry Outputs of 8-bit RCA with Buffers

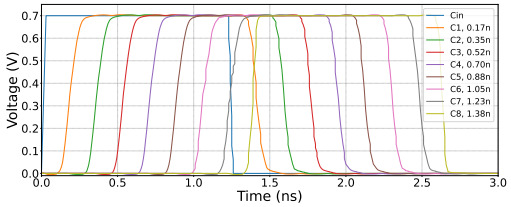

Fig. 6: Delay of Carry Outputs of 8-bit RCA (Mirror Adder Based)

We performed this experiment by cascading 8 FAs to create an 8-bit RCA. The time period of the input signal is set to 3 ns. The waveform of the carry signals for each stage (C1, C2, ..., C8) is shown in Fig. 3. We can see that as the stage count increases, it becomes difficult for the carry signal to reach VDD. This is along the lines of the theoretical delay as shown in Equation (1). To further strengthen our claim we increased the time period of the input from 3 ns to 15 ns to give the carry signal sufficient time to reach VDD. We see that for this case the carry outputs eventually reach VDD as shown in Fig. 4. The delay of C8 is obtained to be 3.54 ns. While this design requires fewer transistors, the delay increases significantly when these designs are cascaded together. Thus, optimizing the number of transistors should not alone be considered, and other metrics should be studied alongside to see the additional costs associated with the design. We will now discuss some strategies that can be used to mitigate such effects but increase the cost of the design.

III. Mitigating Issues with Cascading for RFETs

In this section, we discuss two strategies to reduce the effect of cascading in RFETs.

A. Adding Buffer in the Carry Path

To address the issues discussed in Section II, we propose using buffers to eliminate the effect of RC load accumulation in the carry path. By adding buffer cells in the carry path of the RCA, the RC-ladder is broken and the delay is reduced. However, this reduction comes at the cost of buffers which require 4 RFETs each, i.e., the carry is implemented using 8 RFETs. As a result of this RCA has a lower propagation delay and can operate at a higher frequency. To show the applicability of this method, we performed a transient analysis of the RCA design with buffers. The waveform of the carry signals for each stage when the input signals time period is set to 3 ns as shown in Fig. 3. We observe that each of the carry signals reaches VDD faster than the carry chain without buffers. The delay of C8 is 1.33 ns. Thus, the design is 2.66× faster than the design without buffers. This design can operate with a time period of 3 ns, unlike RCA design without buffers which requires a minimum time period of 15 ns.

B. RCA with RFET-based FA with power rail

We now discuss another mitigation technique to remove the effect of cascading. We implemented a mirror adder-based design of an FA using RFETs [7]. Since this design is based on CMOS, the S/D is connected between VDD/GND, hence there are no issues related to cascading. The carry is implemented using 12 RFETs in the mirror adder. The delay for the C8 is 1.38 ns. Thus, the design is 2.56× faster than the design without buffers. This design can also operate with a time period of 3 ns, similar to the prior technique.

IV. Conclusion and Future Works

In this work, we showed that the current designs that focus on optimizing the area by connecting the S/D to inputs suffer from the issue of delay degradation as a result of cascading. We also discuss two techniques that can mitigate this effect. However, these mitigation techniques come at the cost of an increased number of transistors. We believe that these mitigation techniques can be further optimized leading to more optimal designs which will be explored in the future.

Acknowledgments: The work described in this paper has been supported by the Deutsche Forschungsgemeinschaft (DFG – German Research Foundation) under the priority programme SPP 2253 – 439918011 in project DR 287/38-1.

References

[1] G. Gore *et al.*, "A predictive process design kit for three-independent-gate field-effect transistors," in *VLSI-SoC*, 2019.
[2] J. Trommer *et al.*, "Design enablement flow for circuits with inherent obfuscation based on reconfigurable transistors," in *DATE*, 2023.
[3] N. Kavand *et al.*, "Design of energy-efficient rfet-based exact and approximate 4: 2 compressors and multipliers," *IEEE TCAS II*, 2023.
[4] R. Gauchi *et al.*, "An open-source three-independent-gate fet standard cell library for mixed logic synthesis," in *ISCAS*, 2022.
[5] A. Morgenshtein *et al.*, "Gate-diffusion input (GDI): a power-efficient method for digital combinatorial circuits," *IEEE TVLSI*, 2002.
[6] J. M. Rabaey, *Digital integrated circuits a design perspective*, 1999.
[7] C. K. Jha *et al.*, "Single exact single approximate adders and single exact dual approximate adders," *IEEE TVLSI*, 2023.