

# Optimization-based Test Scheduling for IEEE 1687 Multi-Power Domain Networks Using Boolean Satisfiability

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**Abstract**—The IEEE 1687 Std. provides an efficient access methodology for embedded instruments in complex system-on-a-chip designs by introducing reconfigurable scan networks. This flexibility enables the reduction of the overall test access time, which significantly decreases the test costs compared to the conventional daisy-chaining method. However, the new access methodology strictly requires effective test schedulers that consider multi-power domains with individual constraints.

This work proposes a novel test scheduler that orchestrates the Boolean Satisfiability problem in conjunction with Pseudo-Boolean optimization techniques. The effectiveness of the proposed scheduler is proven by considering networks with over one thousand of so-called instruments forming industrial representative benchmark candidates.

**Index Terms**—Boolean Satisfiability, IEEE 1687, IJTAG, Pseudo-Boolean Optimization, Reconfigurable Scan Networks, Test Scheduling & Scheduling Algorithms

## I. INTRODUCTION

The steadily increasing number of cores in *System-on-a-Chip* (SoC) designs has been boosting the demand for highly efficient instrument access methodologies since the last years. The IEEE 1687 Std. [1] – also known as IJTAG – was introduced to integrate reconfigurable scan networks into SoCs. The faster instruments' access in IJTAG networks is realized by employing a new component called *Segment Insertion Bit* (SIB), which is programmed to include or exclude a section of the network. This principle aims at the scan chain's shortening and, hence, the reduction of the access time overhead. Due to the power, temperature and further system limitations, not all of the SoC's components can be simultaneously tested. A further power demand is introduced when the network components are considered in addition to the instruments' scan and self-test components and, hence, the design is even more prone to issues like IR-drop and test failures [2], [3]. As the overall test time directly affects the test cost, determining an optimized access sequence to the cores massively improves the test procedure and reduces the resulting test costs. Several techniques [4]–[15] have been introduced to reduce the overall test time in IJTAG networks. For example, a formulation for calculating the overall access time is presented in [4]. In work [5], it is tried to minimize the SIB programming overhead by using a hybrid scheduling scheme for instruments with exclusive SIBs. The scan architecture of [7] uses a reconfigurable broadcast mechanism to reduce the overall test data transfer time. A modification scheme for the underlying SIB structures has been proposed in [6] aiming at a higher access bandwidth by introducing a parallel architecture. Boolean satisfiability is exploited in works like [8], [10] to model the reconfigurable scan networks for pattern retargeting and network verification tasks. The SAT-based algorithm of [8] has been further improved in [11] by proposing a new bound calculation method to reduce the number of SAT solver invocations. In particular, significant research has been carried out on the optimization of the test scheduling [12]–[14]. The authors in [13] propose a session-less test scheduling method

by sorting the instruments according to their resource conflict and their number of test patterns. In [14], a pre-emptive scheduling method is introduced, which invokes an exhaustive search over all possible concurrent instruments.

However, all these works do neither consider any power constraints nor incorporate multi-power domains, which is strictly required for an effective test of state-of-the-art SoCs. In [15], a graph-based model of IJTAG networks has been proposed for the first time, which invokes a heuristic method to detect concurrently accessible instruments in multi-power domain IJTAG networks. Although the approach [15] delivers already quite promising results, it is computationally intensive when exploring a huge search space.

In contrast, the proposed scheduling method of this paper is applicable for multi-power domain IJTAG networks embracing ScanMuxes, SCBs, and SIBs regardless of the structure of concurrency groups. This work proposes a novel optimization method using *Boolean Satisfiability* (SAT) in conjunction with *Pseudo-Boolean Optimization* (PBO) techniques. By this, it can be taken advantage of a powerful formal solving engine to, finally, calculate an optimal test schedule yielding highly effective but power-safe tests.

The remainder of this paper is structured as follows: Section II gives a brief introduction to IJTAG, SAT and PBO. Section III describes the proposed formal modeling scheme for IJTAG networks and the SAT-based optimization model. The experimental results are reported in Section IV and, finally, the paper is concluded in Section V.

## II. BACKGROUND

Fig. 1 presents an exemplary IJTAG network named Mingle which is one of the instances of the *ITC'16* benchmark set [16]. This network embraces ten SIBs labeled as  $sib_1$ – $sib_{10}$  and eight instruments indicated by  $w_1$ – $w_8$ , which are connected to the network via parallel *Test Data Registers* (TDRs) performing the read, write and select operations. The elements of the network are divided into three power domains. During a capture operation the network is loaded with data from the instruments through the parallel interface. While this data is transferred to SO, the new scan data, including the network configuration, is shifted in through a shift operation. Finally, an update signal loads the instrument with the new data. This sequence of capture, shift, and update is called a CSU. Typically, the instruments in the network require different number of accesses. As soon as an instrument does not need further access, the corresponding SIB would be closed by resetting its programming bit to 0 during the last scan process. By this, IJTAG provides shorter paths for accessing the rest of instruments in the network.

The SAT problem investigates whether a given Boolean function can be satisfied by a set of assignments to its variables. If such an assignment to all variables exists, the function is classified as *satisfiable* (sat). Otherwise, it is classified as

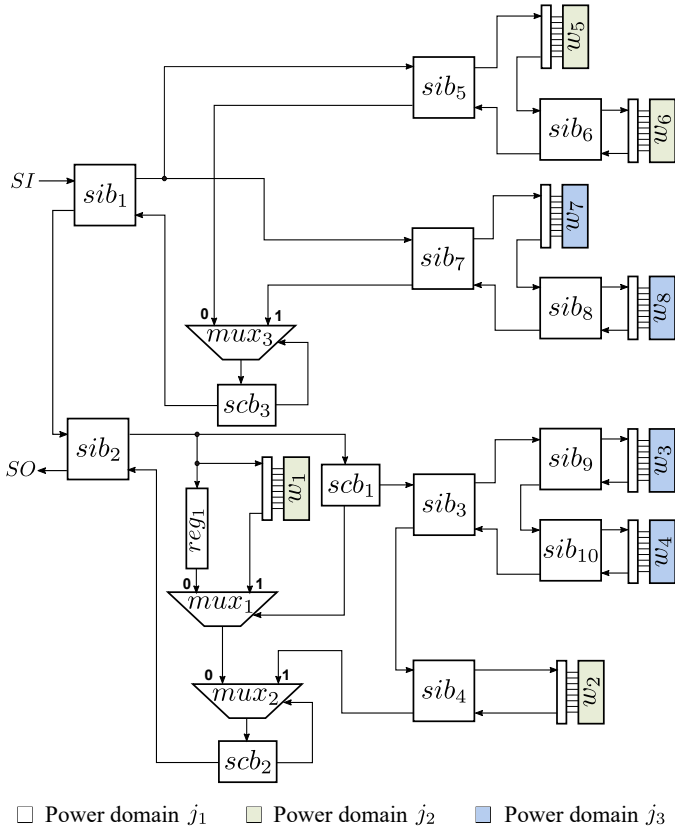


Fig. 1. An exemplary IJTAG network (Mingle) with three power domains

*unsatisfiable* (unsat) [17]. A Boolean function  $\Phi : \{0, 1\}^n \rightarrow \{0, 1\}$  is conventionally represented as *Conjunctive Normal Form* (CNF) forming the SAT instance, which is a conjunction of clauses  $\bigwedge_{i=1}^n c_i$ . A clause is a disjunction of literals  $\bigvee_{i=1}^n \hat{x}_i$  and each literal  $\hat{x}_i$  is either a Boolean variable ( $x$ ) or its negation ( $\bar{x}$ ).

The Pseudo-Boolean (PB) satisfiability problem determines whether a Boolean function  $\Psi : \{0, 1\}^n \rightarrow \{0, 1\}$  with weighted literals can be satisfied by a set of assignments to its variables.

The PBO problem extends the PB-SAT problem such that an objective function  $\mathcal{F}$  is incorporated during the solving process. By this, it is allowed to determine not just a satisfying solution but an optimal one (with respect to a certain optimization criterion, as considered by the objective function). Such an objective function  $\mathcal{F}$  typically invokes the arithmetic sum operation of all PB co-factors and, hence, can be defined as follows:

$$\mathcal{F}(x_1, \dots, x_k) = \sum_{i=1}^k w_i \cdot \hat{x}_i \text{ with } w_1, \dots, w_k \in \mathbb{Z}$$

Modern PBO solving engines support multiple objective functions  $\mathcal{F}_1, \dots, \mathcal{F}_n$ , which are implemented by a prioritized evaluation order. Different PBO-based procedures have already been successfully applied in the testing domain like [18]–[20].

### III. PROPOSED SAT-BASED OPTIMIZATION MODEL

This section presents the proposed model for describing a generic IJTAG network containing instruments, SIBs, SCBs, ScanMuxes and branching nodes. This model is then used to obtain an optimal test schedule per test slice, which covers all instruments within a minimum overall access time without exceeding the power domains' limits. The proposed SAT-based optimization scheme involves the four steps as follows:

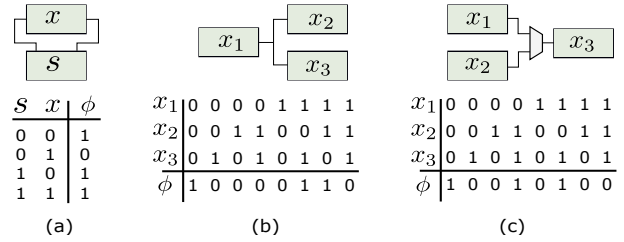


Fig. 2. The structures used in IJTAG network modeling

- 1) Three **building blocks** are introduced allowing for the creation of a highly reduced basic network structure using a (pure) Boolean representation.
- 2) The individual power domain limit is reflected by newly introduced **enumeration constraints**, which invalidate the part of the search space that exceeds the considered power limits.
- 3) One **objective function** is defined, which guides the optimization procedure, i.e., the maximization of the concurrently active instruments.
- 4) The test scheduling process implements an **incremental invocation** of the underlying SAT-solving engine to ensure full coverage of all reachable instruments. The recently covered instruments of test slice  $i-1$  are then masked in the  $i$ -th slice.

#### A. Building Blocks

A serial path between SI and SO may include three main features, namely branching points, merging elements and switching nodes. These features can be combined to create complex hierarchical structures defined by the IEEE 1687 standard. In Fig. 2(a),  $s$  represents a SIB and  $x$  can be another SIB, an instrument or a sub-network. Here, a logical value '1' means that the item is on an active chain and is accessible while a value '0' states that the element cannot be accessed. Since SIBs operate like switches to connect/disconnect the elements of the next hierarchy, in the case that  $s$  is not accessible,  $x$  is neither accessible. However, if  $s$  is accessible – depending on  $s$  being opened or closed –  $x$  will be either accessible or inaccessible. This is expressed by the following equation:

$$\Phi = s \vee \neg x$$

The same CNF is used to model the relation between the wrapped instruments (using negation) and their related TDRs. The models used for branches and multiplexers are derived from the formal models that are used for retargeting and access optimization in [10]. However, in this paper the plain chains are considered as a special case of branches in which the elements have only one successor. Fig. 2(b) presents a branching node with two elements that cannot be placed on a common chain. For a branching node, three features are being considered: At first, only one active chain in an IJTAG network can exist at a time. Therefore, all states that include more than one chain are invalid. This is expressed with the clause  $(\neg x_2 \vee \neg x_3)$ . Secondly, one of the successor nodes must necessarily be on the active chain if a source node is activated. This circumstance is implemented by  $(\neg x_1 \vee x_2 \vee x_3)$ , as stated in Fig. 2(b). Finally, the selection of one node (on a branch) implies that the predecessor is activated, which is reflected by  $(x_1 \vee \neg x_2) \wedge (x_1 \vee \neg x_3)$ . The conjunction of the stated clauses yields the CNF representation of a branching node in the IJTAG network, which can be generalized as follows:

$$\Phi = (\neg x_1 \vee x_2 \cdots \vee x_n) \wedge \bigwedge_{i,j \in \{2..n\} \& i \neq j} (\neg x_i \vee \neg x_j) \wedge \bigwedge_{i=2}^n (x_1 \vee \neg x_i)$$

In a plain chain that is only composed of the elements of the same hierarchy and does not include any branch or

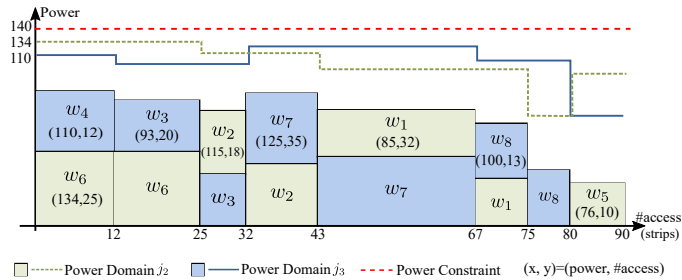


Fig. 3. Power constraint and the result of scheduling for Mingle network

merging node, if one of the components is accessible, the other components on this chain are reachable. Analogously, if one component is not reachable, the other components on the chain are neither reachable. In this case, the stated equation can be reduced to the bi-implication as follows:

$$\Phi = x_1 \leftrightarrow x_2 = (x_1 \vee \neg x_2) \wedge (\neg x_1 \vee x_2)$$

Fig. 2(c) presents the state in which a ScanMux selects between two branches. The CNF for this structure indicates that two inputs cannot be activated at the same time. Furthermore, if one of the inputs is on the active chain, the output has to be on the same chain. On the other hand, the active state of the output implies that one of the inputs is necessarily on the current chain.

These considerations result in the following equation:

$$\Phi = (\neg x_1 \vee \neg x_2) \wedge (\neg x_2 \vee x_3) \wedge (\neg x_1 \vee x_3) \wedge (x_1 \vee x_2 \vee \neg x_3)$$

For a ScanMux with  $n - 1$  inputs and  $x_n$  as output, this equation can be generalized as follows:

$$\Phi = (x_1 \vee x_2 \cdots \vee x_n) \wedge \bigwedge_{i,j \in \{1..n-1\} \& i \neq j} (\neg x_i \vee \neg x_j) \wedge \bigwedge_{i=1}^{n-1} (x_i \vee \neg x_n)$$

After these three building blocks are gradually applied to generate the network model, the test scheduling problem is modeled, as shown in Fig. 3. The horizontal axis is divided to test pattern units. Each strip is assigned to one test pattern, which is applied to the active chain over a CSU and every instrument occupies a number of strips based on its required number of accesses. As long as the access to none of the instruments on the current chain is completed, the path from SI to SO remains unchanged.  $w_4$  and  $w_6$  in Fig. 3 have this condition over the first twelve access. Once the access to these instruments is completed, the new configuration is applied to exclude them from the next scans. The SIB programming bits required for the configuration of the next chain are appended to the test data in each unit. The access to the chains can be reordered and no dependency between them is required.

### B. Enumeration Constraints

The overall power limit  $P_{max,j}$  of each power domain  $j$  is modeled as one enumeration constraint  $\mathcal{C}_j$ , which is added to the overall instance. This follows the basic idea that the accumulated power consumption of (active) instruments should not exceed the domain's power limit during a CSU as follows:

$$\sum_{p_i \in CSU_n} p_i \leq P_{max}$$

More precisely, a Pseudo-Boolean co-factor – the weight  $p$  – is introduced to the Boolean variable  $v$ , which reflects the instrument's activation status while  $p$  represents the weighted (classified) instrument's power consumption. Consequently, a valid solution must fulfill all enumeration constraints:

TABLE I  
BENCHMARK IJTAG NETWORKS

benchmark network	#(nodes, edges)	#instruments	#variables	#clauses
cmplx. name				
B Mingle	(27, 39)	8	35	62
BasicSCB	(33, 42)	5	39	101
TreeFlat	(38, 61)	11	38	107
C q12710	(52, 78)	23	75	102
t512505	(289, 447)	128	417	576
p22810	(520, 789)	242	762	1038
A N17D3	(52, 66)	27	79	144
N32D6	(79, 101)	44	123	216
N73D14	(155, 200)	90	245	426
N132D4	(293, 371)	172	465	825
NE600P150	(1597, 1997)	793	2183	3940
NE1200P430	(3253, 4063)	1629	4502	8202

$$\bigwedge_{\mathcal{C}_{1..j}} \left( \sum_{i \in \mathcal{I}_j} (p_i \cdot v_i) \leq P_{max,j} \right)$$

where  $\mathcal{I}_j$  is the set of reachable instruments of power domain  $j$ . This concept is shown in Fig. 3, in which instruments are organized in two power domains  $j_2$  and  $j_3$ . The sum of instruments' power consumption over strips for domain  $j_2$  and  $j_3$  are shown with dashed and solid lines respectively and each line stays within the limit of its own domain constraint. As the power consumption of the scan chain elements is negligible compared with the one of instruments, it is not considered in Fig. 3.

### C. Objective Functions

The optimization criterion is defined as follows: Let  $I_i(a_i, p_i)$  be the  $i$ -th instrument with  $a_i$  number of accesses and power consumption  $p_i$ . The Pseudo-Boolean objective function  $\mathcal{F}$  addresses the maximization of the allocated power consumption in every strip. To implement  $\mathcal{F}$ , a weight  $p_i$  is added to every of the  $N$  Boolean variable  $v_i$ , representing their power consumption. The weight is accumulated if the instrument is active.  $\mathcal{F}$  is defined as follows:

$$\mathcal{F}(v_1, \dots, v_N) = \sum_{i=1}^N (p_i \cdot v_i)$$

### D. Incremental Invocation

The blocks of Fig. 3 have to be distributed over the strips such that the minimum number of CSUs is required. This is obtained by allocating the maximum power consumption within each strip while observing the concurrent accessibility of the elements. Since no strip initially exists, 1 is assumed for the SI port's corresponding variable. This yields a path to SO including the maximum sum of power consumption such that the active instrument do not violate the power limit, as determined by the SAT solver. The set of instruments that have been activated by the SAT solver are considered as the first strip. The next strip is created when the access to at least one of the instruments (of the current set) has been completed. Accordingly, the corresponding literals are deactivated to discard the already covered instruments in the next run of the solver.

## IV. EXPERIMENTAL RESULTS

This section describes the experimental evaluation of the proposed test scheduler, which is solely written in C++ and utilizes *clasp* (v. 3.1.4) [21] as Pseudo-Boolean optimization solver. All experiments have been tried on different networks from the *ITC'16* benchmark set [16] and conducted on a machine holding an *Intel Xeon E3-1270* processor and 32GB of main memory.

Table I presents rightmost the number of variables and clauses, which have been introduced while processing the individual ICL netlist. The benchmark networks have been classified into three groups of complexity, namely basic,

classic and advanced. The values – being presented as nodes and edges – represent the total number of elements and their connections in the corresponding graphs. These metrics are meant to provide a general overview of the network scale.

Despite being small, the Mingle network [16] contains all structural features like branching and merging points, SIBs, SCBs and parallel branches, as earlier discussed. For the sake of a comprehensible presentation, the experimental evaluation of the proposed test scheduling is described for this network in detail. However, other networks are evaluated as well and their results are briefly summarized in Table II. The Mingle network has artificially been divided into three power domains, as is shown in Fig. 1. Every data path's element is assigned to domain  $j_1$  while the instruments are organized in domains  $j_2$  and  $j_3$ . The power requirements and the number of required accesses are randomly generated and represented as tuples inside the first incidence of each instrument. These values are used as a side-input to the framework, albeit they can be replaced by the real numbers obtained from a power analyzer. As the power domains' limits, 20 for the first domain and 140 for the other two domains have been assumed. The scheduling results are already stated in Fig. 3, in which a sum of 165 accesses is executed in 90 CSUs.

Table II gives the results of the experiments, for which all networks have been divided into three different power domains with individual power limits, analogously to the Mingle network as described above. The table presents the sum of the power consumption in each domain during all accesses. Note that there is not a single violation of the power domains' limits. Additionally, the column #accesses reports the sum of all instruments' accesses in each scenario and column #chains gives the number of required scan chains (test slices) to cover these accesses. The values in column #CSU shows the total number of strips that are required to complete the access to all instruments of the IJTAG network. Finally, the rightmost column presents the CPU time (in seconds) for conducting the complete test scheduling process including the model's creation and the solving process.

## V. CONCLUSION

This paper proposed a novel test scheduler for large IJTAG test networks with multi-power domains by using SAT-based and PBO-based techniques. More precisely, a seamless SAT model for complex IJTAG network structures had been designed, which was then enhanced with Pseudo-Boolean aspects to model specific optimization criteria and enumeration constraints. The scalability of the proposed scheduler was proven by considering even large networks with over one thousand of instruments forming industrial representative benchmark candidates. In the end, the proposed test scheduler allows for determining highly effective but power-safe tests and, by this, contributes to reduced test costs when testing complex and power-critical SoC designs.

## VI. ACKNOWLEDGMENT

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TABLE II  
BENCHMARK RESULTS

network	power domain			#accesses	#CSU	#chains	run-time [s]
	ID	$\sum$ power	limit				
Mingle	1	27	20	165	90	8	0.019
	2	410	140				
	3	428	140				
BasicSCB	1	34	30	88	52	5	0.012
	2	328	180				
	3	473	180				
TreeFlat	1	13	30	158	32	7	0.020
	2	530	330				
	3	412	290				
q12710	1	52	55	377	191	23	0.094
	2	1177	160				
	3	1274	170				
t512505	1	130	30	1684	486	105	3.215
	2	4458	190				
	3	5040	180				
p22810	1	244	30	3090	831	200	12.654
	2	9110	190				
	3	8974	180				
N17D3	1	53	55	488	174	27	0.087
	2	1378	200				
	3	1066	150				
N32D6	1	79	100	655	140	40	0.223
	2	1478	200				
	3	1812	250				
N73D14	1	94	100	900	120	12	0.843
	2	3444	300				
	3	3468	300				
N132D4	1	367	250	2453	380	134	5.008
	2	7059	300				
	3	6487	300				
NE600P150	1	795	500	10524	191	176	159.622
	2	29101	2200				
	3	29441	2300				
NE1200P430	1	1631	700	21187	278	269	555.825
	2	63040	3100				
	3	59358	3300				

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